What is claimed is:

1. A method for forming a gate in a semiconductor device, comprising:

forming a first insulating film and a non-silicide conductive film on a semiconductor substrate;

patterning the first insulating film and the conductive film, to form a gate;

forming a second insulating film thicker than the gate on an entire surface;

planarizing the second insulating film, to expose the gate;

depositing a refractory metal layer on an entire surface such that the refractory metal layer is adjacent to the patterned conductive film;

forming a silicide layer on an upper surface of the gate by heat treatment; and

etching the refractory metal layer and the second insulating film.

2. A method as claimed in claim 1, wherein the refractory metal layer is formed of cobalt.

3. A method as claimed in claim 2, wherein the cobalt is deposited to a thickness of 300Å.

4. A method as claimed in claim 1, further comprising forming gate sidewalls by depositing and etching back an insulating layer after etching the second insulating film to leave an insulating film at sides of the gate.

5. A method as claimed in claim 1, wherein the conductive film is a polysilicon layer.

6. A method as claimed in claim 5, wherein the polysilicon layer has a thickness of 2500Å.

7. A method as claimed in claim 1, wherein the heat treatment for forming the silicide layer is conducted at a temperature of 400 ~ 800°C.

8. A method as claimed in claim 1, wherein the refractory metal layer that does not react is wet etched using H_2SO_4 or HCl-based solution to remove the refractory metal layer.

9. A method as claimed in claim 1, wherein the planarizing includes a chemical mechanical polishing process.

10. A method of fabricating a gate in a semiconductor device, comprising:

forming a non-silicide conductive pattern on a semiconductor substrate; and

forming a silicide pattern on the conductive pattern, the silicide pattern having a predetermined width, and being formed after the conductive pattern is formed, said step of forming a silicide pattern comprising:

forming a refractory metal on the conductive pattern such that the refractory metal is adjacent to the conductive pattern; and

heat treating the refractory metal to form the silicide pattern having the predetermined width at an intersection between the refractory metal and the conductive pattern.

11. The method of claim 10, wherein the conductive pattern is formed of polysilicon.

12. The method of claim 11, wherein the polysilicon pattern has a thickness of 2500 angstroms.

13. The method of claim 11, wherein forming the polysilicon pattern comprises:

forming a polysilicon layer on the semiconductor substrate; and

etching the polysilicon layer to the predetermined width.

14. The method of claim 13, further comprising:

forming an insulating layer on and around the polysilicon pattern; and

planarizing the insulating layer to expose a surface of the polysilicon pattern before forming the refractory metal on the polysilicon layer.

15. The method of claim 14, wherein the refractory metal is cobalt.

16. The method of claim 15, wherein the cobalt is deposited to a thickness of 300 angstroms.

17. The method of claim 13, further comprising:

forming a gate insulating layer on the semiconductor substrate, the polysilicon layer being formed on the gate insulating layer; and

forming a gate insulating pattern by etching the gate insulating layer to the predetermined width.

18. The method of claim 17, wherein the polysilicon layer and the gate insulating layer are respectively etched to form the polysilicon pattern and the gate insulating pattern before the silicide pattern is formed.

19. The method of claim 18, wherein sides of the gate insulating layer, the polysilicon pattern and the silicide pattern are aligned orthogonal to a surface of the semiconductor substrate on which the gate insulating film is formed.

20. The method of claim 19, further comprising:

forming a gate sidewall on at least one side of the gate insulating layer, the polysilicon pattern and the silicide pattern.

21. A method of fabricating a gate electrode of a predetermined width, comprising:

forming a gate insulating layer on a semiconductor substrate; and

forming a silicide pattern on the gate insulating layer without etching a silicide from which the silicide pattern is fabricated.